REMARKS

In the Office Action mailed May 20, 2004:

- Claims 1-7, 10, 19 and 29-37 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention;
- Claims 1-10, 12, 15, 19 and 29-36, as understood, were rejected under 35 U.S.C. 103(a) as being unpatentable over the Miske reference (U.S. Patent 6,163,199).
- Claims 20-28 were allowed;
- Claims 11, 13-14 and 16-18 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims;
- Claim 31 was indicated to be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office Action and to include all of the limitations of the base claim and any intervening claims.

With the entry of this amendment, the pending claims are 1-37.

CLAIM REJECTIONS UNDER 35. U.S.C. 112, SECOND PARAGRAPH

The Examiner correctly points out that the limitation "the input/output supply signal for the logic device" in claim 1 is different from "input/output standards". However, the input/output supply signal for the logic device is neither the reference voltage VREF nor the master control signal VREF_CONTROL, but rather is the logic device's I/O power supply signal VCC_IO as stated at lines 15 and 16 of the first page of the specification. Moreover, the different voltage signals in Miske, such as Vcc, Pvcca, Pvccb, GND, Pgnda and Pgndb, that the Examiner has interpreted as input/output standards, are not input/output standards, but rather are a plurality of control signals that act in concert to connect or disconnect the output node B with the input node A in Fig. 5.

Claim 1 has been amended to recite a logic device that receives an input/output supply signal, thus providing necessary antecedent basis for the limitation "the input/output supply signal received by the logic device". Claims 8, 12 and 29 have likewise been amended to provide appropriate antecedent basis.

There is sufficient support for this amendment in the specification. In particular, the specification, on page 1, lines 15-22, states that a logic device such as a PLD often has multiple power supply signals including, but not limited to:

(1) an input/output supply signal VCC_IO that provides the necessary power for the logic device to drive input/out signals over a system bus, and

(2) a separate internal core power supply signal VCC_INT that is used for processing signals within the logic device.

Independent Claims 1, 8, 12 and 29 have also been revised to clarify that the plurality of standards are input/output standards, as stated for example at page 1, last paragraph of the specification and to avoid use of the term input/output supply signal standards which seems to be causing confusion. The phrase "each having a specified input/output supply signal level" has been deleted as unnecessary in each of these claims. Similar changes have been made in allowed claim 21.

Claim 8 has been amended to recite that the master control signal has a first logic level that is determined by a first supply signal. Support for this amendment can be found in the specification on page 3, lines 11-17. The limitation "a first supply signal" in claim 8 as amended provides necessary antecedent basis for the limitation "the first supply signal" in claim 10.

Claim 29 has been amended to recite "[a] method for selectively providing a reference voltage signal *from a switch circuit* to a logic device ..." and the limitation "supplying a dedicated supply signal to the logic device" has been replaced with "supplying a dedicated supply signal to *the switch circuit*".

The Examiner contends that claim 37 appears to be misdescriptive since applicants' Fig. 1 shows T5 being conductive while T1 and T2 are non-conductive at the same instant. Applicants respectfully disagree.

Claim 37 is directed to an embodiment in which the master control signal VREF_CONTROL is low, the transmission switch circuit 110 is off, and the reference voltage signal VREF is not passed to the input buffers 140 of the logic device. In this case, there is no need for the dedicated power supply signal VCC_DED to be different from the input/output supply signal VCC_IO. Therefore, the dedicated power supply signal VCC_DED may be shorted to the input/output supply signal VCC_IO. *See* page 10, lines 7-11 of the specification.

In view of the foregoing comments and amendments, applicants submit that claims 1-7, 10, 19 and 29-37 are definite under 35 U.S.C. 112, second paragraph.

CLAIM REJECTIONS UNDER 35. U.S.C. 103(a)

The Examiner has rejected claims 1-10, 12, 15, 19 and 29-36, as understood, under 35 U.S.C. 103(a) as being unpatentable over the Miske reference (U.S. Patent 6,163,199). Applicants respectfully traverse the rejections.

Applicants' claim 1 recites in pertinent part "a switch circuit for selectively providing a reference voltage signal to *a logic device...operable in accordance with any one of a plurality of input/output standards,* wherein at least one of the plurality of input/output standards is a voltage referenced standard, the switch circuit comprising a transmission switch circuit...in response to a first control signal, the first control signal having a logic level determined by *a dedicated supply signal, that is different from the input/output supply signal for the logic device*".

Applicants' specification (page 1, line 23 - page 2, line 14) discusses in details that some logic devices, e.g., PLDs, may have a same set of I/O terminals supporting multiple I/O standards. In this case, a switch circuit is required in order to pass a particular reference voltage signal to an I/O terminal if the terminal is operated under the voltage-referenced standard and block the reference voltage signal if the terminal is operated under other standards. Since the I/O supply signal VCC_IO powering the switch circuit may be too low for a particular voltage-referenced standard, a dedicated supply signal different from the I/O power supply is required for the operation of the switch circuit under such a voltage-referenced standard.

Miske, however, does not disclose a logic device operable in accordance with a plurality of input/output standards. Indeed, the Examiner, on page 4 of the Office action, has acknowledged that Miske does not disclose a logic device coupled to the output of the switching circuit at all. Miske teaches an overvoltage/undervoltage tolerant transfer gate for passing a logic signal from an input node to an output node.

Miske provides seven exemplary operating scenarios of the transfer gate 10 in Fig. 4 (col.7, line 51-col. 9, line 28) and illustrates how the different control signals, such as Vcc, Pvcca, Pvccb, GND, Pgnda and Pgndb, coordinate with each other to pass the logic signal from node A to node B. For example, the first scenario is that OEN = 0.4V, Vcc = 3.0V and the voltage at node A = 0.4V. According to Fig. 5, a low voltage (0.4V) at node A turns off transistor M4 and turns on transistor M5 causing rail Pvcca to be charged to Vcc through M5. A low voltage (OEN=0.4V) at the input of inverter I16 causes the transistor M2's gate terminal to be charged to Vcc. Similarly, the output of inverter I13 is also charged to Vcc,

causing the outputs of inverters I14 and I15 to discharge the gates of transistors M0 and M1 to GND. As a result, node B is discharged to approximately 0.4V by transistor M2 alone since the voltage at node A is sufficiently low to pinch off transistor M0. A low voltage at node B also enables rail Pvccb to be charged to Vcc. In other words, the voltage configuration at OEN, Vcc, GND and node A determines the voltages at Pvcca, Pvccb, Pgnda and Pgndb, and they are not equivalent to the plurality of input/output standards recited in applicants' claim 1.

Furthermore, contrary to the Examiner's contention, rail Pgndb of Miske is not a dedicated supply signal recited in claim 1. Rather, it has the lower potential of either GND or node B (see Fig.7 and col. 7, lines 18-20) depending on which transistor, M9 or M10, is on. In other words, Pgndb cannot be greater than GND or 0V and it provides a ground reference voltage for inverter I17. Therefore, the output of inverter I17 that the Examiner has equated to the first control signal is not determined by Pgndb, but by the input of I17 which is OEN.

In summary, Miske does not disclose a switch circuit as required by the recitation in claim 1 that "selectively provid[es] a reference voltage signal to a logic device that ... is operable in accordance with any one of a plurality of input/output standards ...". Likewise, Miske does not disclose a first control signal as required by the recitation in claim 1 that "ha[s] a logic level determined by a dedicated supply signal...".

Since Miske does not teach each limitation recited in claim 1, claim 1 as well as its dependent claims 2-7 and 19 are patentable over Miske. Claims 8, 12 and 29, as well as their respective dependent claims, each recite at least substantially the same set of limitations recited in claim 1 and are therefore patentable for at least the same reasons.

In view of the foregoing, applicants believe that all of the claims are now in condition for allowance and respectfully request the Examiner to pass the subject application to issue. If for any reason the Examiner believes any of the claims are not in condition for allowance, he is encouraged to phone the undersigned at (212) 309-6632 so that any remaining issues may be resolved.

Respectfully submitted,

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Francis E. Morris 24,615
Francis E. Morris (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
101 Park Avenue
New York, NY 10178
(212) 309-6632